CLAIMS

What is claimed is:

1. A method for processing an instruction within a processor, the method comprising:

executing an instruction within the processor, wherein the processor processes a plurality of types of interruptions, wherein the processor comprises a plurality of interruption resources, and wherein a type of interruption can be associated with a specific interruption resource; and

in response to receiving an interruption, saving processor state information into an interruption resource based on a type for the received interruption.

2. The method of claim 1 further comprising:

in response to saving processing state information into the interruption resource, invoking an interruption handler to process the received interruption.

3. The method of claim 1 wherein the types of interruptions comprise aborts, faults, interrupts, and traps.

4. The method of claim 1 wherein the plurality of interruption resources comprises a plurality of sets of interruption control registers.

5. The method of claim 1 further comprising:

holding concurrently multiple sets of processor state information in multiple interruption resources.

6. The method of claim 1 further comprising:

saving a first set of processor state information into a first interruption resource in response to receiving a first interruption, wherein the first interruption is a first type of interruption; and

prior to restoring the first set of processor state information, saving a second set of processor state information into a second interruption resource in response to receiving a second interruption, wherein the second interruption is a second type of interruption.

7. The method of claim 6 wherein the first interruption is an interrupt, and wherein the second interruption is a trap.

8. The method of claim 6 wherein the second interruption is a single-step trap.

9. A method for processing an instruction within a processor, the method comprising:

executing an instruction within the processor, wherein the processor comprises a plurality of interruption resources for saving processor state;

saving a first set of processor state information into a first interruption resource in response to receiving a first interruption; and

prior to restoring the first set of processor state information, saving a second set of processor state information into a second interruption resource in response to receiving a second interruption.

10. The method of claim 9 further comprising:

maintaining a single-step trap mode while executing instructions within an interruption handler.

11. A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

means for fetching instructions from memory;

means for executing an instruction within the processor

means for processing a plurality of types of interruptions;

a plurality of interruption resources, wherein a type of interruption can be associated with a specific interruption resource; and

means for saving, in response to receiving an interruption, processor state information into an interruption resource based on a type for the received interruption.

12. The processor of claim 11 further comprising:

means for invoking an interruption handler to process the received interruption in response to saving processing state information into the interruption resource.

13. The processor of claim 11 wherein the types of interruptions comprise aborts, faults, interrupts, and traps.

14. The processor of claim 11 wherein the plurality of interruption resources comprises a plurality of sets of interruption control registers.

15. A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

an instruction execution unit;

a first interruption resource for saving processor state;

a second interruption resource for saving processor state;

first saving means for saving a first set of processor state information into the first interruption resource in response to receiving a first interruption; and

second saving means for saving a second set of processor state information into the second interruption resource in response to receiving a second interruption prior to restoring the first set of processor state information.

16. The processor of claim 15 further comprising:

means for maintaining a single-step trap mode while executing instructions within an interruption handler.

17. The processor of claim 15 wherein the first interruption resource is a set of one or more registers and wherein the second interruption resource is a set of one or more registers.

18. A computer program product in a computer-readable medium for use in a data processing system for processing an instruction within a processor, the computer program product comprising:

means for executing an instruction within the processor, wherein the processor processes a plurality of types of interruptions, wherein the processor comprises a plurality of interruption resources, and wherein a type of interruption can be associated with a specific interruption resource; and

means for saving, in response to receiving an interruption, processor state information into an interruption resource based on a type for the received interruption.

19. The computer program product of claim 18 further comprising:

means for invoking an interruption handler to process the received interruption in response to saving processing state information into the interruption resource.

20. The computer program product of claim 18 wherein the types of interruptions comprise aborts, faults, interrupts, and traps.

21. The computer program product of claim 18 wherein the plurality of interruption resources comprises a plurality of sets of interruption control registers.

22. The computer program product of claim 18 further comprising:

means for saving a first set of processor state information into a first interruption resource in response to receiving a first interruption, wherein the first interruption is a first type of interruption; and

means for saving, prior to restoring the first set of processor state information, a second set of processor state information into a second interruption resource in response to receiving a second interruption, wherein the second interruption is a second type of interruption.

23. The computer program product of claim 22 wherein the first interruption is an interrupt, and wherein the second interruption is a trap.

24. The computer program product of claim 22 wherein the second interruption is a single-step trap.

25. A computer program product in a computer-readable medium for use in a data processing system for processing an instruction within a processor, the computer program product comprising:

means for executing an instruction within the processor, wherein the processor comprises a plurality of interruption resources for saving processor state;

means for saving a first set of processor state information into a first interruption resource in response to receiving a first interruption; and

means for saving a second set of processor state information into a second interruption resource in response to receiving a second interruption prior to restoring the first set of processor state information,

26. The computer program product of claim 25 further comprising:

means for maintaining a single-step trap mode while executing instructions within an interruption handler.